Interface Circuits for the QD Series Quadrature Demodulators

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INTRODUCTION

The QD series quadrature demodulators provide exceptional linearity and demodulation accuracy for direct conversion and low-IF receiver applications. This application note presents several circuit ideas for interfacing the differential I/Q outputs of the QD series demodulators to single-ended loads and modern differential A/D converters.

DEMODULATOR PORTS

Figure 1 shows the block diagram of a QD series demodulator. For proper operation, the demodulator should be supplied with an LO drive signal having a power level within the demodulator's specified LO power range. The LO signal should have low 2nd harmonic content to achieve the rated LO-RF isolation. The LO and RF ports are single-ended and matched to 50 Ω.

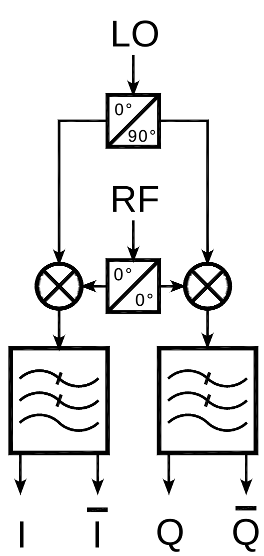

Figure 1. Quadrature Demodulator Block Diagram

The two differential I/Q output ports, $I/\overline{I}$ and $Q/\overline{Q}$, each have 100 Ω differential source impedance. Internally matched lowpass filters on the I/Q ports limit the demodulator's noise bandwidth.

The I/Q outputs can be modeled as voltage sources with 100 Ω of differential source resistance. When a sinewave RF input signal at +3 dBm is demodulated, the resulting I and Q differential output signals are approximately 400 mV p-p centered at 0 V (ground). This is equivalent to four single-ended baseband outputs supplying –10 dBm each into a 50 Ω single-ended load.

To minimize amplitude imbalance and quadrature phase error, the baseband outputs should be terminated into a matched load impedance over the processed frequency bandwidth. The DC voltage offset present at each baseband output is typically within a few mV of ground and may be blocked with DC-blocking capacitors without degrading demodulator performance.

INTERFACING TO SINGLE-ENDED LOADS

A simple differential-to-single-ended amplifier circuit based on the Analog Devices[1] AD8130 is shown in Figure 2. This circuit converts differential I and Q outputs from a QD series demodulator into single-ended I and Q signals capable of driving low-impedance loads. The V_o input provides a means of level-shifting the I and Q signals to any convenient DC voltage level. This circuit has excellent amplitude and phase tracking from DC to 100 MHz.

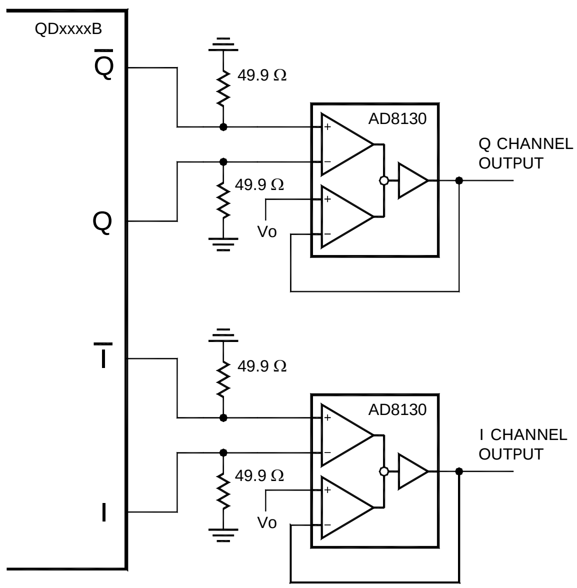

Figure 2. Active Interface to Single-Ended Loads

The transformer circuit shown in Figure 3 provides an all-passive method of converting the differential I and Q outputs from a QD series demodulator into single-ended outputs. Since this method is AC-coupled, it cannot be used in applications that require I and Q DC response. The DC-blocking capacitors prevent self-modulation and degraded IIP2 performance.

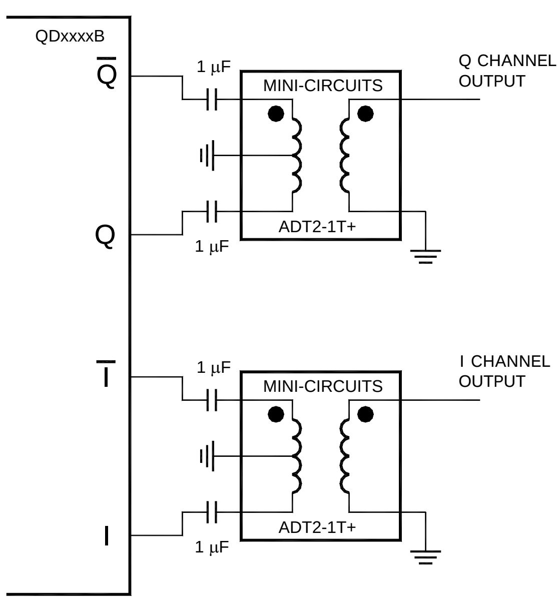

Figure 3. Transformer Circuit to Single-Ended Loads

The transformer interface of Figure 3 has excellent amplitude and phase tracking from 100 kHz to over 300 MHz. It can drive 50 Ω single-ended loads with less than 1 dB of insertion loss.

DUAL A/D CONVERTER INTERFACE

In many direct conversion and low-IF receivers, the baseband I and Q outputs from the QD series demodulators must be amplified and lowpass filtered before digitization. The QD series demodulator's I and Q differential outputs often must also be level-shifted to the A/D converter's positive reference voltage. The differential amplifier circuit shown in Figure 4 provides +14 dB gain and has a lowpass cutoff of 30 MHz. It also moves the common-mode voltage to the A/D converter's reference voltage (V_{ref}). The gain of the Analog Devices[2] AD8132 differential amplifier is set by the ratio of the feedback resistor to the series input resistor. A 30 MHz differential lowpass filter is formed by the output resistors and capacitors.

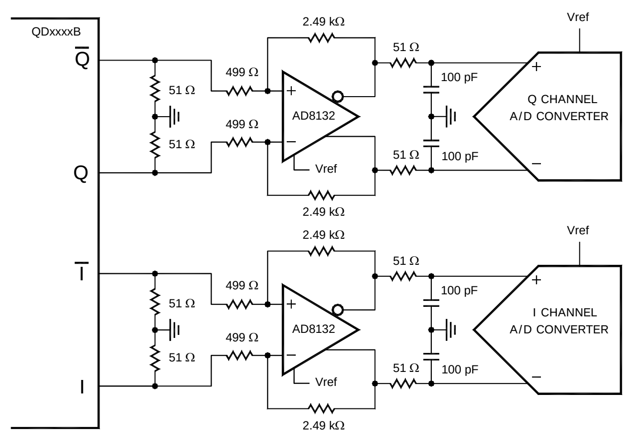

Figure 4. A/D Converter Interface

REFERENCES

[1] Analog Devices, Inc., "AD8129/*AD8130 Product Datasheet, Rev. 0*", 2001.

[2] Analog Devices, Inc., "*AD8132 Product Datasheet, Rev. C*", 2003.